REMARKS

In response to the Office Action mailed October 3, 2005, Applicants respectfully request reconsideration.

Claims 1-30 were previously pending in this application. By this amendment, Applicants amend claims 10, 13, 19, 23 and 25 solely for clarification. As a result, claims 1-30 are pending for examination, of which claims 1, 24, 26, and 30 are independent. No new matter has been added.

Applicants' lack of response to any of the contentions set forth in the Office Action should not be construed as Applicants' acquiescence to any such contentions, as Applicants only respond to contentions to the extent Applicants believe is necessary to place all of the claims in condition for allowance.

1. Priority

Applicants have requested a certified copy of the priority patent application from the European Patent Office and will submit the certified copy when it is received.

2. The Objections to the Title, Abstract and Written Description Have Been Overcome

In response to the objections to the Title and Abstract, Applicants have amended Title and Abstract as shown above on pages 2 and 3. Accordingly, Applicants respectfully request that the objections to the Title and Abstract be withdrawn. Further, in response to the objection to page 6, line 2, Applicants have changed "10 000" to --ten thousand-- . Accordingly, Applicants respectfully request that the objection to the written description be withdrawn.

3. The Objections to the Claims are Overcome

In response to the objections to claims 13 and 25, each of claims 13 and 25 have been amended as shown above to change "different signal" to --a signal--. Accordingly, Applicants respectfully request that the objections to claims 13 and 25 be withdrawn.

4. Claims 1-23 Patentably Distinguish Over Baker

Claim 1 stands rejected under §102(b) as purportedly being anticipated by U.S. Patent No. 6,434,649 (Baker). Applicants respectfully traverse this rejection.

Baker is directed towards a data transfer arrangement mechanism employed to transfer data to various components of a data processor. (Col. 1, line 4-7). In describing the disadvantages of prior art arrangements, Baker refers to the controller of U.S. Patent No. 5,668,965, indicating that the controller forms a three-way connection of three kinds of busses. (Col. 1, lines 24-36).

Baker describes a multimedia processor 100, which is a fully programmable chip that handles concurrent operations. Because all the main components of the processor are disposed on one chip set, the throughput of the system is remarkably better than those of conventional system. (col. 4, lines 48-58). The multimedia processor 100 includes arbiters 140, 142, and 144, which each include FIFOs, and includes a data streamer 122. Baker describes a data bus master as "a component that requests to accomplish an operation," whereas a data bus slave is a component that responds to a request. (Col. 7, lines 14-18).

In contrast to Baker, Claim 1 recites:

> A processing system for accessing first and second data types, the first data type being data supplied from a peripheral and the second data type being randomly accessible data held in a data memory, the processing system comprising:
>
> a processor for executing instructions;
>
> **a stream register unit connected to supply data from the peripheral to the processor;**
>
> **a FIFO connected to receive data from the peripheral and connected to the stream register unit by a communication path, along which the said data can be supplied from the FIFO to the stream register unit; and**
>
> a memory bus connected between the data memory and the processor, across which the processor can access the randomly accessible data.

Preliminarily, the rejection of claim 1 under §102(b) is improper because the rejection does not establish a single system including all of the limitations recited in claim 1. The Office Action rejects claims 1 based on disclosure found in col. 1, lines 24-36 and col. 7, lines 6-11. Column1 describes prior art bus systems including a controller that forms a three-way connection of three kinds of busses. The remainder of column 1 (lines 37-67) discuss the disadvantages of these prior art systems. Column 7 describes the system proposed by Baker to alleviate these problems. Thus, the disclosures from columns 1 and 7 are for different systems.

These cited passages do not disclose a processing system, as recited in claim 1, but disparate pieces of separate systems. As the cited passages do not teach or suggest a single processing system that includes all of the limitations recited in claim 1, the rejection of claim 1 under §102(b) set forth in the Office Action is improper.

Further, even if the cited passages from column 1 and column 7 described parts of a same system, claim1 would distinguish over such systems. Baker does not disclose or suggest the processing system for accessing first and second data types recited in claim 1. Particularly, Baker does not disclose or suggest a stream registry unit connected to supply data from the peripheral to the processor, nor and a FIFO connected to receive data from the peripheral and connect it to the stream registry unit by a communication path, along which the said data can be supplied from the FIFO to the stream registry unit, as required by claim 1. The Office Action contends that such a stream register unit is disclosed in column 1, lines 24-36 and column 7, lines 6-11. However, as noted above, this passage describes a three-way connection of three kinds of buses, and makes no mention of a stream register. Further, although Baker discloses a data streamer 122, this data streamer is not connected to supply data from a peripheral to a processor. Rather, the data streamer 122 operates exclusively via an input/output bus 132. The Office Action also contends that a stream register is the equivalent of a data bus master described in Baker. However, this is simply not true. As noted above, Baker discloses that a data bus master is "a component that requests to accomplish an operation." Under no reasonable interpretation is this the same thing as a stream registry unit connected to supply data from a peripheral to a processor. With respect to the FIFO recited in claim 1, column 7, lines 6-11 of Baker merely describe bus arbiters that include FIFOs. However, there is no teaching in Baker that these FIFOs are connected to a stream registry unit by a communication path, along which data can be supplied from the FIFO to the stream registry unit, as required by claim 1. Thus, Baker does not teach the combination of the stream registry unit and FIFO recited in claim 1.

In view of the foregoing, Applicants respectfully request that the rejection of claim 1 under §102(b) be withdrawn. Claims 2-23 each depend from claim 1 and are patentable for at least the same reasons. Accordingly, Applicants request that the rejections of these claims under §102(b) be withdrawn.

5. Claims 24 and 25 Patentably Distinguish Over Baker

Claim 24 stands rejected under §102(b) as purportedly being anticipated by Baker. Applicants respectfully traverse this rejection.

Claim 24 recites:

> A streaming data handling system, comprising :
> a processor;
> a stream register associated with the processor;
> a FIFO memory connected to the processor via the stream register,
> **wherein the stream register and the FIFO operate the same data handling protocol such that the stream register can receive streamed data items from the FIFO memory and supply them to the processor in the received order.**

It should be clear from the discussion of Baker set forth above, Baker does not teach or suggest all of the limitations of the stream data handling system recited in claim 24, including a stream register that can receive streamed data items from a FIFO memory and supply them to a processor in the received order, as required by claim 24. Further, Baker does not disclose a stream register and a FIFO that operate the same data handling protocol. The Office Action contends that either column 1, lines 24-36 or column 7, lines 6-11 disclose this limitation of claim 24. However, these passages are silent regarding the use of data handling protocols, let alone that a stream registry and a FIFO use the same one.

In view of the foregoing, claim 24 patentably distinguishes over Baker. Accordingly, Applicants respectfully request that the rejection of claim 24 under §102(b) be withdrawn. Claim 25 depends from claim 24 and is patentable for at least the same reasons. Accordingly, Applicants respectfully request that the rejection of claim 25 be withdrawn.

6. Claims 26-29 Patentably Distinguish Over Baker

Claim 26 stands rejected under §102(b) as purportedly being anticipated by Baker. Applicants respectfully traverse this rejection.

Claim 26 recites:

> A stream register connectable between a processor and a peripheral, the stream register comprising :
> a receiver arranged to receive a request for a data item from the processor; and
> a stream engine, arranged to send the request to the peripheral and receive one or more signals back from the peripheral indicating availability of the requested data item,

and, if the data item is available, send the data item to the processor and **if the data item is not available, send a timeout signal to the processor.**

Baker does not or suggest the stream register recited in claim 26, in particular, a stream engine arranged to send a time-out signal to a processor if a data item is not available, as required by claim 26. The Office Action contends that this is disclosed in column 12, lines 36-46. However, this cited passage merely discusses the exchange of signals between a request bus master and a request bus slave, and makes no mention of a time-out signal in relation to a stream engine or otherwise. In relation to claim 15, the Office Action asserts that column 24, lines 21-53 disclose a time-out generator. However, this cited passage makes no mention of generating a time-out, but rather, discloses determining the bandwidth of a data transfer based on channel priority and minimum inter-burst delay, among other things.

In view of the foregoing, claim 26 patentably distinguishes over Baker. Accordingly, Applicants respectfully request that the rejection of claim 26 under §102(b) be withdrawn. Claims 27-29 each depend from claim 26 and are patentable for at least for the same reasons. Accordingly, Applicants respectfully request that the rejections of these claims under §102(b) be withdrawn.

7. Claim 30 Patentably Distinguishes Over Baker

Claim 30 stands rejected under §102(b) as purportedly being anticipated by Baker. Applicants respectfully traverse this rejection.

Claim 30 recites:

A stream register connectable between a processor and a memory, the stream register comprising :

a receiver arranged to receive a request for a data item from the processor; and a stream engine, arranged to send the request to the memory and receive one or more signals back from the memory indicating availability of the requested data item, and, if the data item is available, send the data item to the processor and **if the data item is not available, send a stall signal to the processor.**

Claim 30 patentably distinguishes over Baker because Baker does not teach or suggest the stream register including all of the limitations recited in claim 30, in particular, a stream

engine arranged to send a stall signal to a processor if a data item is not available. The Office Action contends that such a stream engine is disclosed in column 12, lines 35-46. However, as noted above, this passage merely recites the exchange of communication signals between a request bus master and a request bus slave, and does not mention sending a stall signal to a processor by a stream engine or otherwise. Further, the Office Action contends, in relation to claim 11, that column 24, lines 24-67 of Baker disclose a stream register arranged to send a stall signal to a processor. However, this cited passage does not teach such a stream register, but rather discusses how much data can be transferred from a particular schedule channel before a different channel is scheduled for service.

In view of the foregoing, claim 30 patentably distinguishes over Baker. Accordingly, Applicants respectfully request that the rejection of claim 30 under §102(b) be withdrawn.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicants hereby request any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,

By: _____

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